## Features

- Compatible with MCS-51™ Products
- 1 Kbyte of Reprogrammable Flash Memory
  Endurance: 1,000 Write/Erase Cycles
- 2.7 V to 6 V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Two-Level Program Memory Lock
- 64 bytes SRAM
- 15 Programmable I/O Lines
- One 16-Bit Timer/Counter
- Three Interrupt Sources
- Direct LED Drive Outputs
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes

# 8-Bit Microcontroller with 1 Kbyte Flash

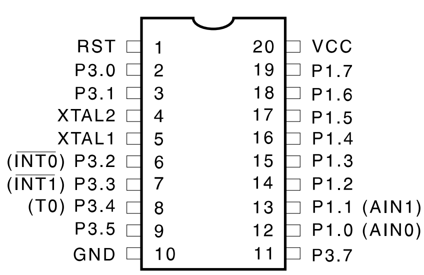
## Description

The AT89C1051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 1 Kbyte of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C1051 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C1051 provides the following standard features: 1 Kbyte of Flash, 64 bytes of RAM, 15 I/O lines, one 16-bit timer/counter, a three vector two-level interrupt architecture, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C1051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

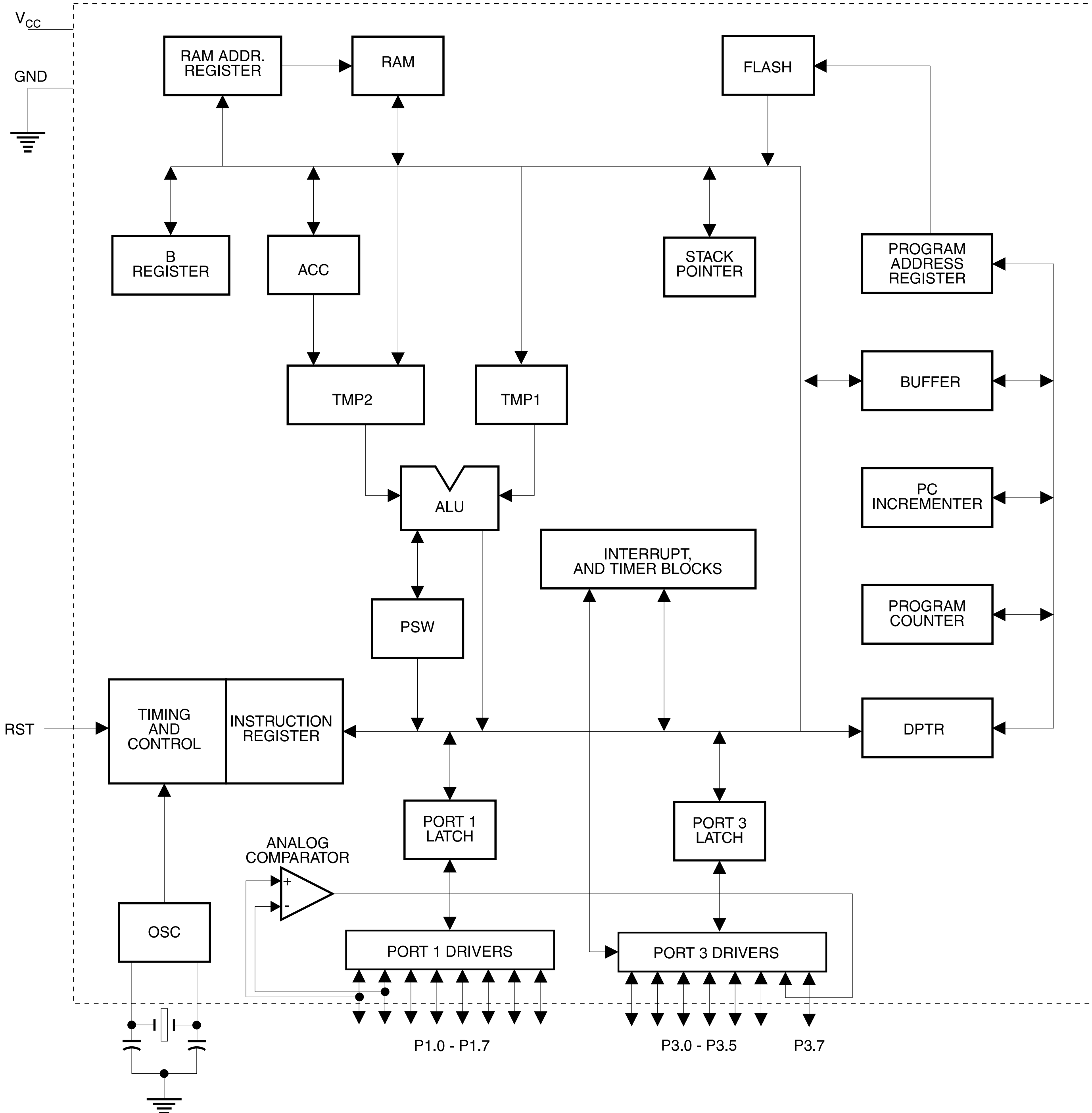
## Pin Configuration

PDIP/SOIC




0366C

## Block Diagram



## Pin Description

$V_{CC}$

Supply voltage.

GND

Ground.

Port 1

Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (IIL) because of the internal pullups.

Port 1 also receives code data during Flash programming and program verification.

Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bidirectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C1051 as listed below:

| Port Pin | Alternate Functions |
|---|---|
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

Each machine cycle takes 12 oscillator or clock cycles.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

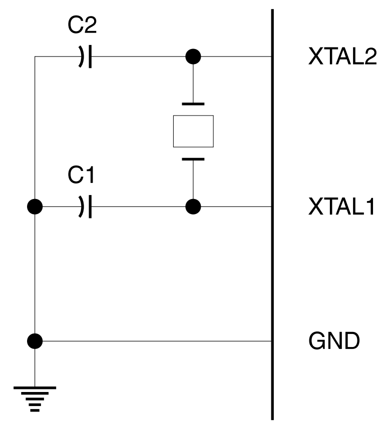
XTAL2

Output from the inverting oscillator amplifier.

## Oscillator Characteristics

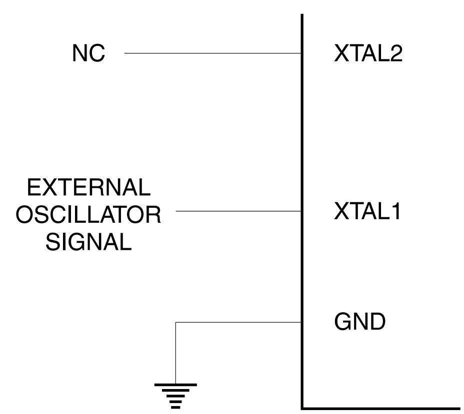
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Figure 1.** Oscillator Connections




Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

**Figure 2.** External Clock Drive Configuration



## Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the table below.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

**Table 1.** AT89C1051 SFR Map and Reset Values

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0F8H | | | | | | | | | 0FFH |
| 0F0H | B<br>00000000 | | | | | | | | 0F7H |
| 0E8H | | | | | | | | | 0EFH |
| 0E0H | ACC<br>00000000 | | | | | | | | 0E7H |
| 0D8H | | | | | | | | | 0DFH |
| 0D0H | PSW<br>00000000 | | | | | | | | 0D7H |
| 0C8H | | | | | | | | | 0CFH |
| 0C0H | | | | | | | | | 0C7H |
| 0B8H | IP<br>XXX00000 | | | | | | | | 0BFH |
| 0B0H | P3<br>11111111 | | | | | | | | 0B7H |
| 0A8H | IE<br>0XX00000 | | | | | | | | 0AFH |
| 0A0H | | | | | | | | | 0A7H |
| 98H | | | | | | | | | 9FH |
| 90H | P1<br>11111111 | | | | | | | | 97H |
| 88H | TCON<br>00000000 | TMOD<br>00000000 | TL0<br>00000000 | | TH0<br>00000000 | | | | 8FH |
| 80H | | SP<br>00000111 | DPL<br>00000000 | DPH<br>00000000 | | | | PCON<br>0XXX0000 | 87H |

## Restrictions on Certain Instructions

The AT89C1051 is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 1 Kbyte of flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 1K for the AT89C1051. This should be the responsibility of the software programmer. For example, LJMP 3FEH would be a valid instruction for the AT89C1051 (with 1K of memory), whereas LJMP 410H would not.

1. Branching instructions:

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 3FFH for the 89C1051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ With these conditional branching instructions the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

2. MOVX-related instructions, Data Memory:

The AT89C1051 contains 64 bytes of internal data memory. Thus, in the AT89C1051 the stack depth is limited to 64 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

## Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

## Lock Bit Protection Modes[1]

| Program Lock Bits | | | |
|---|---|---|---|
| | LB1 | LB2 | Protection Type |
| 1 | U | U | No program lock features. |
| 2 | P | U | Further programming of the Flash is disabled. |
| 3 | P | P | Same as mode 2, also verify is disabled. |

Note: 1. The Lock Bits can only be erased with the Chip Erase operation

## Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

P1.0 and P1.1 should be set to ’0’ if no external pullups are used, or set to ’1’ if external pullups are used.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

## Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

P1.0 and P1.1 should be set to ’0’ if no external pullups are used, or set to ’1’ if external pullups are used.

## Programming The Flash

The AT89C1051 is shipped with the 1 Kbyte of on-chip PEROM code memory array in the erased state (i.e., contents = FFH) and ready to be programmed. The code memory array is programmed one byte at a time. *Once the array is programmed, to re-program any non-blank byte, the entire memory array needs to be erased electrically.*

**Internal Address Counter:** The AT89C1051 contains an internal PEROM address counter which is always reset to 000H on the rising edge of RST and is advanced by applying a positive going pulse to pin XTAL1.

**Programming Algorithm:** To program the AT89C1051, the following sequence is recommended.

1. Power-up sequence:
   Apply power between $V_{CC}$ and GND pins
   Set RST and XTAL1 to GND
   With all other pins floating, wait for greater than 10 milliseconds
2. Set pin RST to ’H’
   Set pin P3.2 to ’H’
3. Apply the appropriate combination of ’H’ or ’L’ logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the PEROM Programming Modes table.

To Program and Verify the Array:

4. Apply data for Code byte at location 000H to P1.0 to P1.7.
5. Raise RST to 12V to enable programming.
6. Pulse P3.2 once to program a byte in the PEROM array or the lock bits. The byte-write cycle is self-timed and typically takes 1.2 ms.
7. To verify the programmed data, lower RST from 12V to logic ’H’ level and set pins P3.3 to P3.7 to the appropiate levels. Output data can be read at the port P1 pins.
8. To program a byte at the next address location, pulse XTAL1 pin once to advance the internal address counter. Apply new data to the port P1 pins.
9. Repeat steps 5 through 8, changing data and advancing the address counter for the entire 1 Kbyte array or until the end of the object file is reached.
10. Power-off sequence:
    set XTAL1 to ’L’
    set RST to ’L’
    Float all other I/O pins
    Turn Vcc power off

**Data Polling:** The AT89C1051 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P1.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

**Ready/Busy:** The Progress of byte programming can also be monitored by the RDY/BSY output signal. Pin P3.1 is pulled low after P3.2 goes High during programming to indicate BUSY. P3.1 is pulled High again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed code data can be read back via the data lines for verification:

1. Reset the internal address counter to 000H by bringing RST from 'L' to 'H'.
2. Apply the appropriate control signals for Read Code data and read the output data at the port P1 pins.
3. Pulse pin XTAL1 once to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat steps 3 and 4 until the entire array is read.

The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire PEROM array (1 Kbyte) and the two Lock Bits are erased electrically by using the proper combination of control signals and by holding P3.2 low for 10 ms. The code array is written with all "1"s in the Chip Erase operation and must be executed before any non-blank memory byte can be re-programmed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 000H, 001H, and 002H, except that P3.5 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(001H) = 11H indicates 89C1051

## Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

## Flash Programming Modes

| Mode | | RST | P3.2/PROG | P3.3 | P3.4 | P3.5 | P3.7 |
|---|---|---|---|---|---|---|---|
| Write Code Data(1,3) | | 12V | ‾_/‾ | L | H | H | H |
| Read Code Data(1) | | H | H | L | L | H | H |
| Write Lock | Bit - 1 | 12V | ‾_/‾ | H | H | H | H |
| | Bit - 2 | 12V | ‾_/‾ | H | H | L | L |
| Chip Erase | | 12V | ‾_/‾(2) | H | L | L | L |
| Read Signature Byte | | H | H | L | L | L | L |

Notes: 1. The internal PEROM address counter is reset to 000H on the rising edge of RST and is advanced by a positive pulse at XTAL1 pin.
2. Chip Erase requires a 10 ms PROG pulse.
3. P3.1 is pulled Low during programming to indicate RDY/BSY.

**Figure 3.** Programming the Flash Memory

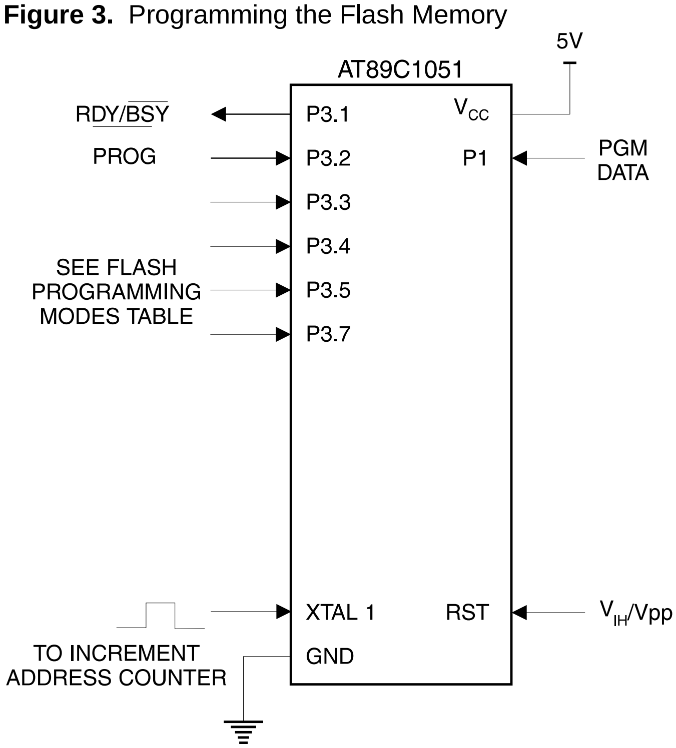
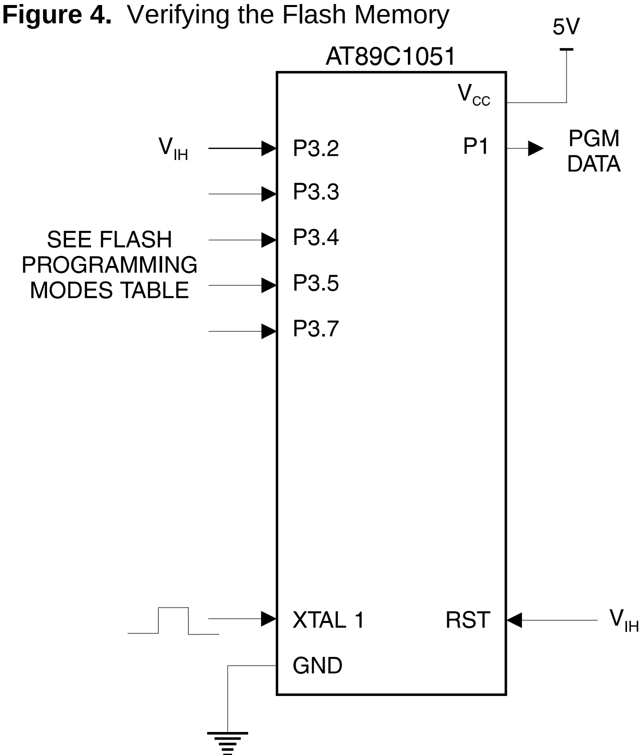



**Figure 4.** Verifying the Flash Memory



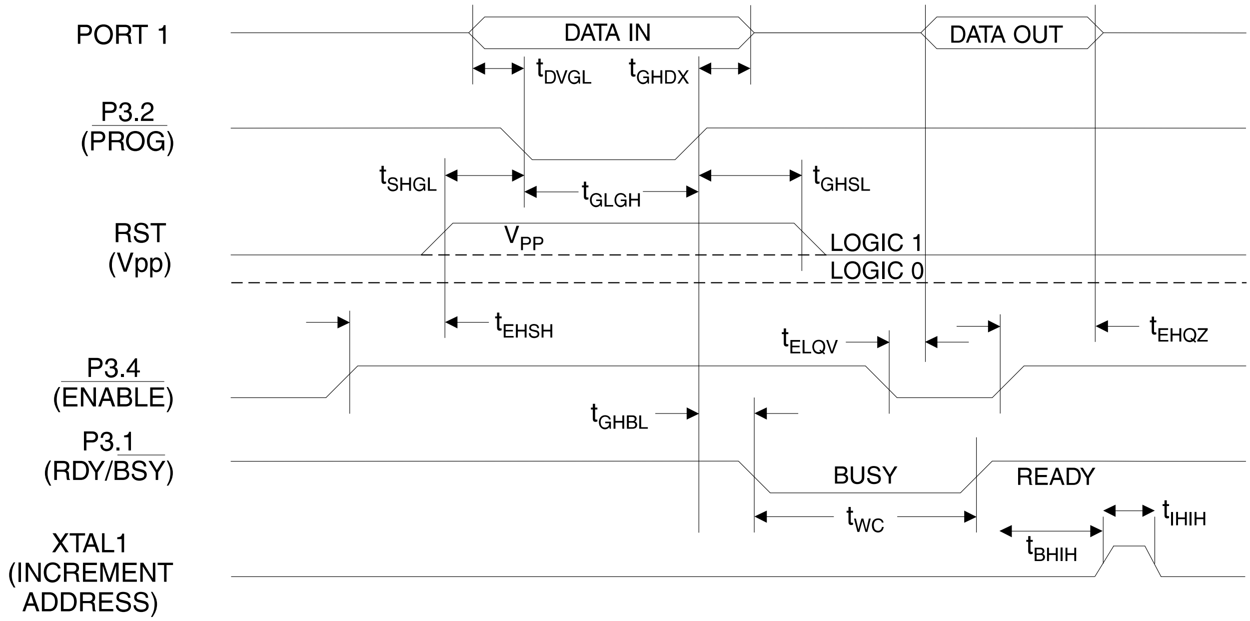

## Flash Programming and Verification Characteristics

$T_A$ = 21°C to 27°C, $V_{CC}$ = 5.0 ± 10%

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Enable Voltage | 11.5 | 12.5 | V |
| $I_{PP}$ | Programming Enable Current | | 250 | µA |
| $t_{DVGL}$ | Data Setup to $\overline{PROG}$ Low | 1.0 | | µs |
| $t_{GHDX}$ | Data Hold After $\overline{PROG}$ | 1.0 | | µs |
| $t_{EHSH}$ | P3.4 ($\overline{ENABLE}$) High to $V_{PP}$ | 1.0 | | µs |
| $t_{SHGL}$ | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| $t_{GHSL}$ | $V_{PP}$ Hold After $\overline{PROG}$ | 10 | | µs |
| $t_{GLGH}$ | $\overline{PROG}$ Width | 1 | 110 | µs |
| $t_{ELQV}$ | $\overline{ENABLE}$ Low to Data Valid | | 1.0 | µs |
| $t_{EHQZ}$ | Data Float After $\overline{ENABLE}$ | 0 | 1.0 | µs |
| $t_{GHBL}$ | $\overline{PROG}$ High to $\overline{BUSY}$ Low | | 50 | ns |
| $t_{WC}$ | Byte Write Cycle Time | | 2.0 | ms |
| $t_{BHIH}$ | RDY/$\overline{BSY}$ to Increment Clock Delay | 1.0 | | µs |
| $t_{IHIL}$ | Increment Clock High | 200 | | ns |

Note: 1. Only used in 12-volt programming mode.

## Flash Programming and Verification Waveforms




## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -1.0 V to +7.0 V |
| Maximum Operating Voltage | 6.6 V |
| DC Output Current | 25.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

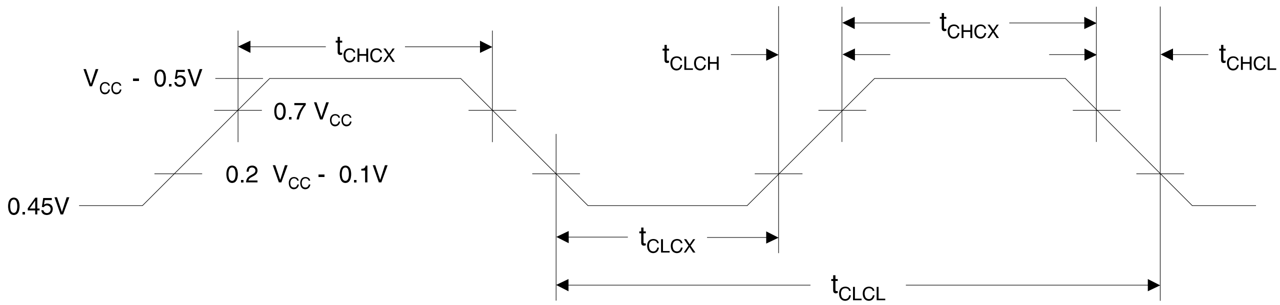
## D.C. Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 2.7 V to 6.0 V (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | -0.5 | 0.2 $V_{CC}$-0.1 | V |
| $V_{IH}$ | Input High Voltage | (Except XTAL1, RST) | 0.2 $V_{CC}$+0.9 | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input High Voltage | (XTAL1, RST) | 0.7 $V_{CC}$ | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output Low Voltage(1) (Ports 1, 3) | $I_{OL}$ = 20 mA, $V_{CC}$ = 5 V<br>$I_{OL}$ = 10 mA, $V_{CC}$ = 2.7 V | | 0.50 | V |
| $V_{OH}$ | Output High Voltage (Ports 1, 3) | $I_{OH}$ = -80 µA, $V_{CC}$ = 5 V ± 10% | 2.4 | | V |
| | | $I_{OH}$ = -30 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -12 µA | 0.9 $V_{CC}$ | | V |
| $I_{IL}$ | Logical 0 Input Current (Ports 1, 2, 3) | $V_{IN}$ = 0.45 V | | -50 | µA |
| $I_{TL}$ | Logical 1 to 0 Transition Current (Ports 1, 2, 3) | $V_{IN}$ = 2 V | | -750 | µA |
| $I_{LI}$ | Input Leakage Current (Port P1.0, P1.1) | 0 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| $V_{OS}$ | Comparator Input Offset Voltage | $V_{CC}$ = 5 V | | 20 | mV |
| $V_{CM}$ | Comparator Input Common Mode Voltage | | 0 | $V_{CC}$ | V |
| RRST | Reset Pulldown Resistor | | 50 | 300 | KΩ |
| $C_{IO}$ | Pin Capacitance | Test Freq. = 1 MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{CC}$ | Power Supply Current | Active Mode, 12 MHz, $V_{CC}$ = 6 V/3 V | | 15/5.5 | mA |
| | | Idle Mode, 12 MHz, $V_{CC}$ = 6 V/3 V<br>P1.0 & P1.1 = 0V or $V_{CC}$ | | 5/1 | mA |
| | Power Down Mode(2) | $V_{CC}$ = 6 V P1.0 & P1.1 = 0V or $V_{CC}$ | | 100 | µA |
| | | $V_{CC}$ = 3 V P1.0 & P1.1 = 0V or $V_{CC}$ | | 20 | µA |

Notes: 1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
Maximum $I_{OL}$ per port pin:20 mA
Maximum total IOL for all output pins:80 mA
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum $V_{CC}$ for Power Down is 2 V.

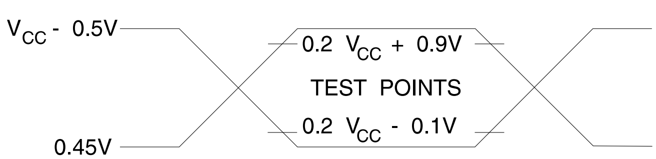
## External Clock Drive Waveforms




## External Clock Drive

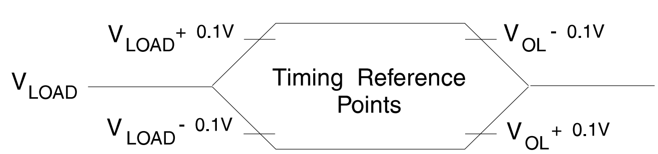
| Symbol | Parameter | $V_{CC}$ = 2.7 V to 6.0 V | | $V_{CC}$ = 4.0 V to 6.0 V | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 12 | 0 | 24 | MHz |
| $t_{CLCL}$ | Clock Period | 83.3 | | 41.6 | | ns |
| $t_{CHCX}$ | High Time | 30 | | 15 | | ns |
| $t_{CLCX}$ | Low Time | 30 | | 15 | | ns |
| $t_{CLCH}$ | Rise Time | | 20 | | 20 | ns |
| $t_{CHCL}$ | Fall Time | | 20 | | 20 | ns |

## AC Testing Input/Output Waveforms (1)




Note: 1. AC Inputs during testing are driven at $V_{CC}$ - 0.5 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at $V_{IH}$ min. for a logic 1 and $V_{IL}$ max. for a logic 0.

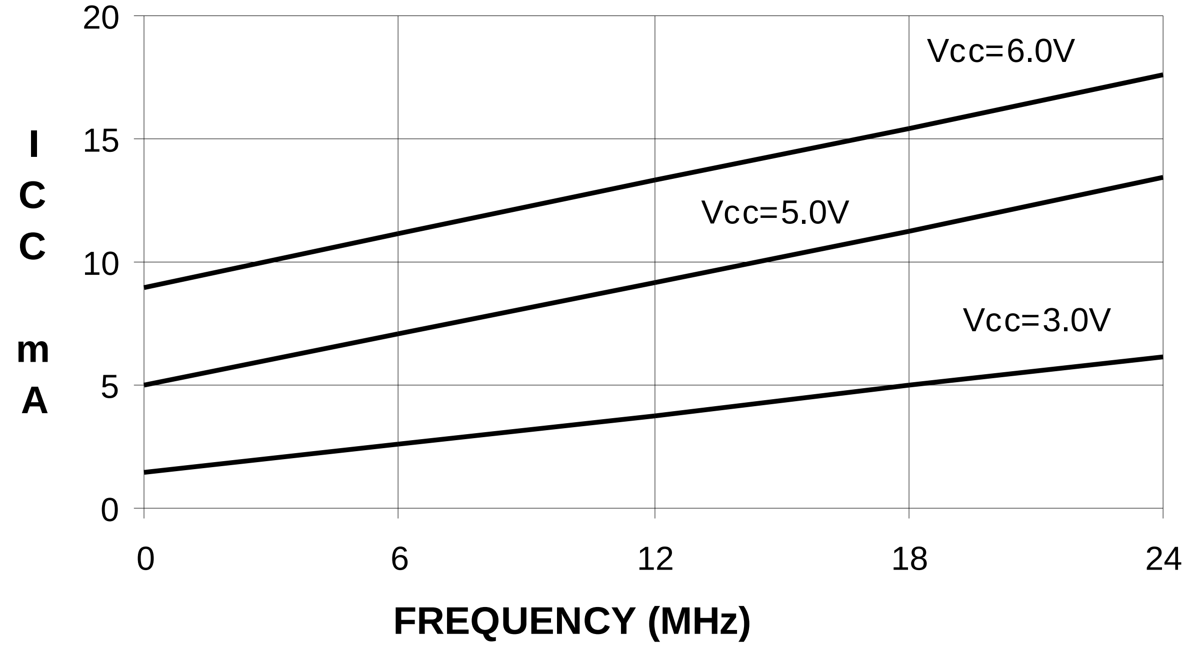
## Float Waveforms (1)




Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs.

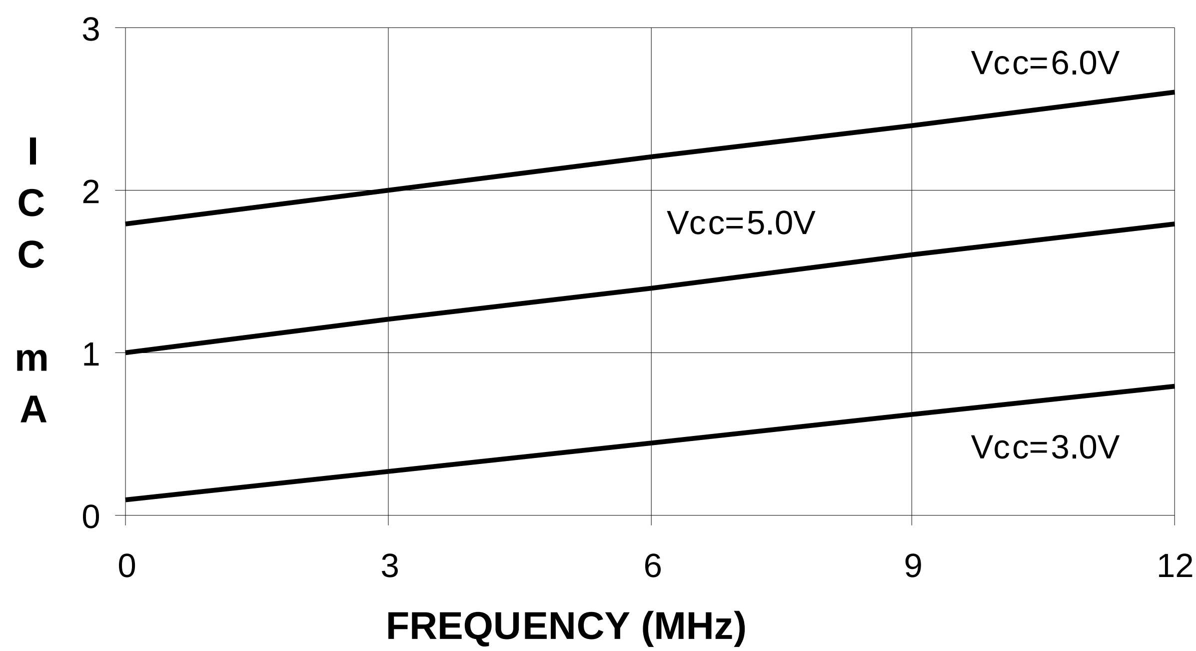
# AT89C1051

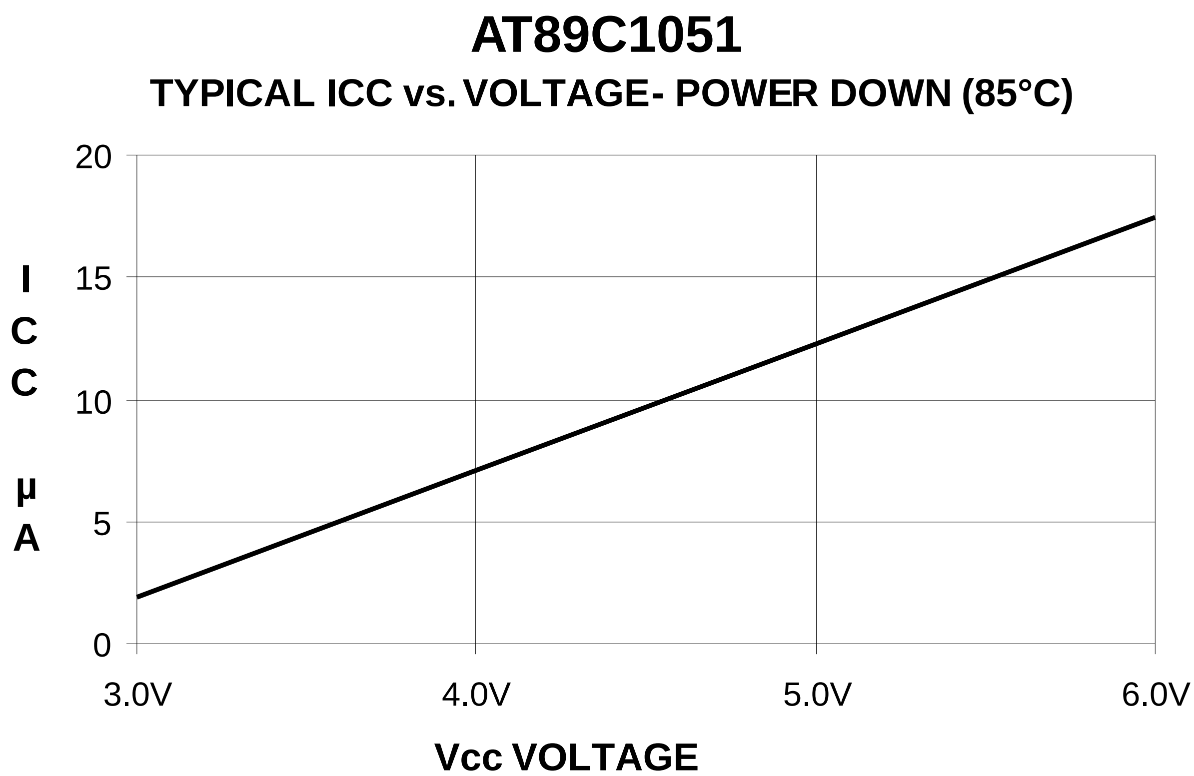
## TYPICAL ICC - ACTIVE (85°C)




# AT89C1051

## TYPICAL ICC - IDLE (85°C)






Note: 1. XTAL1 tied to GND for $I_{CC}$ (power down).
2. P.1.0 and P1.1 = $V_{CC}$ or GND.
3. Lock bits programmed.

## Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 12 | 2.7 V to 6.0 V | AT89C1051-12PC<br>AT89C1051-12SC | 20P3<br>20S | Commercial<br>(0°C to 70°C) |
| | | AT89C1051-12PI<br>AT89C1051-12SI | 20P3<br>20S | Industrial<br>(-40°C to 85°C) |
| 24 | 4.0 V to 6.0 V | AT89C1051-24PC<br>AT89C1051-24SC | 20P3<br>20S | Commercial<br>(0°C to 70°C) |
| | | AT89C1051-24PI<br>AT89C1051-24SI | 20P3<br>20S | Industrial<br>(-40°C to 85°C) |

| Package Type | |
|---|---|
| **20P3** | 20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **20S** | 20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |